intended to be descriptive and illustrative with the goal of facilitating comprehension, but are not intended to be limiting with respect to the scope of the inventions as recited in the claims. Each such definition is intended to also capture additional equivalent items, technologies or terms that would be known or would become known to a person having ordinary skill in this art as equivalent or otherwise interchangeable with the respective item, technology or term so defined. Unless otherwise required by the context, the verb "may" indicates a possibility that the respective action, step or implementation may be performed or achieved, but is not intended to establish a requirement that such action, step or implementation must be performed or must occur, or that the respective action, step or implementation must be performed or achieved in the exact manner described.

[0059] The above description is illustrative and not restrictive. This patent describes in detail various embodiments and implementations of the present invention, and the present invention is open to additional embodiments and implementations, further modifications, and alternative constructions. There is no intention in this patent to limit the invention to the particular embodiments and implementations disclosed; on the contrary, this patent is intended to cover all modifications, equivalents and alternative embodiments and implementations that fall within the scope of the claims. Moreover, embodiments illustrated in the figures may be used in various combinations. Any limitations of the invention should, therefore, be determined not with reference to the above description, but instead should be determined with reference to the appended claims along with their full scope of equivalents.

What is claimed is:

1. A Field Effect Transistor device comprising:

a compound semiconductor layer;

a first and second source finger disposed on a surface of the compound semiconductor material;

a first and second drain finger disposed on the surface of the compound semiconductor material, and alternating with the first and second source finger;

a plurality of gate fingers disposed on the surface of the compound semiconductor material, each gate finger between an adjacent source finger and drain finger and having a first and second end, the first end of each gate finger electrically coupled to a gate signal through a first pad and the second end of each gate finger electrically coupled to the gate signal through a second pad;

a plurality of first source vias distributed along a width of the first source finger and a plurality of second source vias distributed along a width of the second source finger, the first and second source vias configured to partition source current along the width of the first and second source finger, respectively;

a plurality of source conductors distributed along the width of the first and second source finger, each source conductor in electrical contact with the first source finger through at least one of the first source vias and with the second source finger through at least one of the second source vias;

a plurality of first drain vias distributed along a width of the first drain finger and a plurality of second drain vias distributed along a width of the second drain finger, the first and second drain vias configured to partition drain current along the width of the first and second drain finger, respectively; and

a plurality of drain conductors distributed along the width of the first and second drain finger, each drain conductor in electrical contact with the first drain finger through at least one of the first drain vias and with the second drain finger through at least one of the second drain vias.

2. The Field Effect Transistor device of claim **1**, further comprising an insulation layer disposed between the source conductors and the source fingers and between the drain conductors and the drain fingers, the source vias and the drain vias embedded in the insulation layer.

3. The Field Effect Transistor device of claim **1**, wherein the length of the first and second source finger is less than about 7 microns.

4. The Field Effect Transistor device of claim **1**, wherein the length of the plurality of gate fingers is less than about 0.5 microns.

5. The Field Effect Transistor device of claim **1**, wherein the length of a region of the first source finger proximate a via is greater than the length of a region of the first source finger between vias.

6. The Field Effect Transistor device of claim **1**, wherein the source conductors are about normal to the source fingers.

7. The Field Effect Transistor device of claim **6**, wherein the drain conductors are about parallel to the source conductors.

8. The Field Effect Transistor device of claim **1**, wherein the pitch of the gate fingers is less than about 15 microns.

9. The Field Effect Transistor device of claim **1**, wherein compound semiconductor material is gallium arsenide or gallium nitride.

10. The Field Effect Transistor device of claim **1**, wherein the sum of the width of the gate fingers is greater than about 1.0 meters.

11. The Field Effect Transistor device of claim **1**, wherein an average separation between the first source vias distributed along the width of the first source finger is less than about 10 microns.

12. A method for switching current using a Field Effect Transistor, the method comprising:

partitioning source current into a plurality of source current segments for distribution along a width of a source element of the Field Effect Transistor;

distributing the plurality of source current segments to sections of the source element through a plurality of source electrodes, each electrode in electrical contact with at least one of a plurality of vias distributed along a surface of the source element;

partitioning drain current into a plurality of drain current segments for distribution along a width of a drain element of the Field Effect Transistor, the drain element disposed adjacent the source element;

distributing the plurality of drain current segments to sections of the drain element through a plurality of drain electrodes, each electrode in electrical contact with at least one of a plurality of vias distributed along a surface of the drain element;

coupling a gate signal to a first and second end of a gate finger disposed between the adjacent source and gate elements; and

switching current between the source element and the drain element using the gate signal coupled to the ends of the gate finger.